

PATENT

REMARKS

This paper is responsive to Final Office Action dated January 5, 2005. Claims 1-30 were examined. Applicant has not amended any of the claims and respectfully traverses all rejections.

Rejection Under 35 U.S.C. §103

Claims 1-8, 10-22 and 25-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over "A Lock-Free Multiprocessor OS Kernel" by Massalin (hereinafter "Massalin") in view of U.S. Patent No. 6,651,146 issued to Srinivas (hereinafter "Srinivas"). Claims 9, 23 and 24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Massalin in view of Srinivas further in view of U.S. Patent No. 6,581,063 issued to Kirkman (hereinafter "Kirkman"). Applicant traverses all rejections based on 1) the Office's failure to respond to many of Applicant's arguments from the previous response of 2 September 2004, and 2) defective §103 rejections.

Failure to Respond to Previous Arguments

Applicant provided arguments specifically referring to claims 1, 4, 6, 7, 14, 15, 25, and 29. Although the Office asserts that new grounds for rejections are provided in the current Final Office Action, the new art of record only addressed some of the previous arguments by Applicant.

Applicant previously argued that Massalin fails to anticipate limitations of claims 1 and 25 that recite linearizable operations. Applicant made the following arguments:

With regard to claims 1 and 25, *Massalin* does not disclose or suggest "linearizable operations to define semantics of at least insert and remove operations" as recited in claim 1 or "wherein instances of the functional sequences are linearizable" as recited in claim 25. *Although linearizable and atomic are not the same, despite the assertions in the Office Action, Massalin does not disclose linearizable operations or atomic operations for insertion and removal of values from a concurrent shared object. Massalin states that "[t]he main difficulty with linked list traversal is that nodes can disappear while visiting them" (page 6, section 3.3), which fails linearizability and atomicity. Massalin proposes an alternative, which is utilizing a binary marker to restrict access. This binary marker technique is essentially a locking technique, thus blocking (page 6, section 3.3). However, claim 1 recites a "non-blocking concurrent shared object" and claim 25 recites "at least two functional sequences providing non-blocking access to a concurrent shared object."*

## PATENT

Srinivas does not disclose or suggest linearizability, and the Office does not contend that Srinivas discloses such subject matter. Applicant respectfully requests that the Office respond to the previously asserted arguments that are reiterated herein.

Applicant also argued in the previous response that Massalin failed to disclose or suggest traversing an encoded group without use of an atomic operation as recited in claim 29, and similarly recited in claims 6 and 7. The following is a portion of the previously asserted argument:

***The traversal code in Massalin includes a CAS2 instruction, which is an atomic instruction (Figure 3). The Office Action refers to the 4<sup>th</sup> full paragraph of page 3, which discloses separation of a run queue traversal and the queue element update. On page 6, in section 3.3., Massalin specifically states that a 2-word Compare-and-Swap is utilized to set a mark in the run-queues implementation upon entering a node, which occurs during traversal of a linked-list of nodes.***

In the previous Office Action, Massalin was relied upon to reject claims 6 and 7, while Agesen was relied upon to reject claim 29. The Office did not respond to Applicant's arguments and the new art of record does not address these arguments. In fact, the rejections of claims 6 and 7 have not changed at all from the previous Office Action. Moreover, the rejection of claim 7 refers to sections of Massalin that provide no indication of the number of atomic operations for insertions or deletions of an element. Claim 7 specifically recites "at most, one atomic update" for successful completion of an insert, and "at most, two atomic updates" for successful completion of a deletion. With regard to claim 29, the Office's rejection uses the same language from the previous Office Action, but replaces cites to Agesen with cites to Massalin, even though the cites to Massalin do not disclose or suggest "means for traversing the encoded group without use of an atomic operation" as recited in claim 29. The quote from Massalin relied upon by the Office is the following: "we separate the run-queue traversal (done lock-free, safely, and concurrently) from the queue element update (done locally)." This quoted portion of Massalin does not disclose or suggest claim 29. Applicant respectfully requests the Office to indicate where Massalin discloses traversing an encoded group without use of an atomic operation.

The Office also failed to respond to arguments for claims 4, 14, and 15. Again, the Office recycles the rejection of claims 14 and 15 from the previous Office Action without modification and without replying to Applicant's arguments. For claim 4, the Office simply

## PATENT

inserts a cite to Srinivas in the previous rejection language. However, the cited section of Srinivas does not disclose or suggest "wherein reclamation of storage associated with the excised node is independent of the linearizable operations" as recited in claim 4. The Office relies on the statement from Massalin that the run-queue traversal is separate from the queue element update. The cited section from Srinivas is the following:

List managers are software routines that can vary depending on the types of lists managed and the defined management process. In one embodiment of the present invention a list is managed primarily with operations employed to add elements to and remove elements from a list. In particular, embodiments of the present invention employ the following functions; "add a data element to the front of a list" (ATLF), "add an element to the back of a list" (ATLB) and "remove a data element from the front of a list" (RFLF), each function implemented using an atomic operation of a CAS and as disclosed enable management of a list of the present invention in an SMP system without the use of locks. In one embodiment of the ATLF, an ATLB and an RFLF, on a singly linked list of free memory data elements, allows improved memory/cache management in an SMP system.

Applicant respectfully requests for the Office to indicate what portion of this cited section of Srinivas and what section of Massalin discloses claim 4. Applicant also respectfully requests for the Office to indicate what section of Massalin is being interpreted by the Office as disclosing claims 14 and 15, thus allowing Applicant to respond properly, because the currently relied upon section of Massalin does not disclose or suggest these claims. Arguments from the previous response for claims 14 and 15 are reproduced below.

With regard to claim 14, the Office Action assumes without any support that a binary marker, if characterizable as a distinguishing bit value, is in an unused portion of a next node pointer of the logically deleted node. ***Nothing in the section cited by the Office Action indicates where the binary marker is located. The relied upon section of Massalin only states "[w]e set the mark at the same time we enter the node using a two-word Compare-and-Swap."***

With regard to claim 15, ***the Office Action states that a "two-word Compare-and-Swap can guarantee safety by simultaneously checking the previous node's pointer."*** Neither the statement in the Office Action nor Massalin discloses or suggests utilizing any levels of indirection and especially does not disclose or suggest "the marked node indication includes a distinguishing additional level of indirection between the next node point of the logically deleted node and a respective other one of the nodes" as recited in claim 15.

PATENT

Defective §103 Rejections


Applicant respectfully submits that the §103 rejections of Applicant's claims are defective. The additional disclosure of Srinivas does not provide any additional support for the rejections, and the Office cannot simply swap Massalin's 2CAS with a CAS. Massalin already includes disclosure of a CAS instruction, and the Office does not even attempt to rely on Srinivas for anything more than disclosure of the CAS instruction. Since Massalin already disclosed a CAS instruction, the additional disclosure of a CAS instruction in Srinivas is duplicative. The Office attempts to simply replace the 2CAS of Massalin with a CAS from Srinivas, and nothing more. Attempting to simply swap instructions trivializes the complexities of code disclosed in Massalin and trivializes Applicant's claimed invention. Merely swapping the 2CAS of Massalin with a CAS does not achieve Applicant's claimed invention, and both the implementation and the result of such a change is unknown. The Office assumes that replacing a 2CAS, which operates with 2 reference values, 2 new values, and 2 targets, can simply be replaced with a CAS, which operates with 1 reference value, 1 new value, and 1 target. There is no indication of how such swapping can be implemented and how it will affect Massalin's techniques.

Neither Massalin nor Srinivas discloses or suggests using a single target synchronization primitive that atomically examines and updates a node to logically delete the node from a concurrent shared object. None of the art or record discloses or suggests independent claims 1, 16, 25, or 29. Neither Massalin, Srinivas, nor Kirkman, standing alone or in combination, disclose or suggest any of Applicant's claims for at least the reasons above. In addition, all of the dependent claims are at least allowable because their corresponding base claims are allowable.

Conclusion

In summary, claims 1 – 30 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

PATENT

<b>CERTIFICATE OF MAILING OR TRANSMISSION</b>	
I hereby certify that, on the date shown below, this correspondence is being	
<input type="checkbox"/>	deposited with the US Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
<input checked="" type="checkbox"/>	facsimile transmitted to the US Patent and Trademark Office.
 Steven R. Gilliam	7-Mar-2005 Date

Respectfully submitted,



Steven R. Gilliam, Reg. No. 51,734  
Attorney for Applicant(s)  
(512) 338-6320  
(512) 338-6301 (fax)

<b>EXPRESS MAIL LABEL:</b> _____
----------------------------------